INSTITUTE VISION

"To be a preferred institution in Engineering Education by achieving excellence in teaching and research and to remain as a source of pride for its commitment to holistic development of individual and society"

INSTITUTE MISSION

"To continuously strive for the overall development of students, educating them in a state of the art infrastructure, by retaining the best practices, people and inspire them to imbibe real time problem solving skills, leadership qualities, human values and societal commitments, so that they emerge as competent professionals"

DEPARTMENTAL VISION

“To be the centre of excellence in providing education in the field of Electronics and Communication Engineering to produce technically competent and socially responsible engineering graduates.”

DEPARTMENTAL MISSION

“Educating students to prepare them for professional competencies in the broader areas of the Electronics and Communication Engineering field by inculcating analytical skills, research abilities and encouraging culture of continuous learning for solving real time problems using modern tool”.

PROGRAM EDUCATIONAL OBJECTIVES (PEOs):

PEO1:

Acquire core competence in Applied Science, Mathematics, and Electronics and Communication Engineering fundamentals to excel in professional carrier and higher study.

PEO2:

Design, Demonstrate and Analyze the Electronic Systems which are useful to society.

PEO3:

Maintain Professional and Ethical values, Employability skills, Multidisciplinary approach and an Ability to realize Engineering issues to broader social contest by engaging in lifelong learning.

PROGRAM SPECIFIC OUTCOMES(PSOS)

The graduates will be able to:

PSO1:

An ability to understand the concepts of Basic Electronics and Communication Engineering and to apply them to various areas like Signal Processing, VLSI, Embedded Systems, Communication Systems and Digital & Analog Devices

PSO2:

An ability to solve complex Electronics and Communication Engineering problems, using latest hardware and software tools, along with analytical skills to arrive at cost effective and appropriate solutions

PROGRAM OUTCOMES(POs):

1. **Engineering knowledge**: Apply the knowledge of mathematics, science, engineering fundamentals, and an engineering specialization to the solution of complex engineering problems.
2. **Problem analysis**: Identify, formulate, review research literature, and analyze complex engineering problems reaching substantiated conclusions using first principles of mathematics, natural sciences, and engineering sciences.
3. **Design/development of solutions**: Design solutions for complex engineering problems and design system components or processes that meet the specified needs with appropriate consideration for the public health and safety, and the cultural, societal, and environmental considerations.
4. **Conduct investigations of complex problems**: Use research-based knowledge and research methods including design of experiments, analysis and interpretation of data, and synthesis of the information to provide valid conclusions.

5. **Modern tool usage**: Create, select, and apply appropriate techniques, resources, and modern engineering and IT tools including prediction and modeling to complex engineering activities with an understanding of the limitations.
6. **The engineer and society**: Apply reasoning informed by the contextual knowledge to assess societal, health, safety, legal and cultural issues and the consequent responsibilities relevant to the professional engineering practice.
7. **Environment and sustainability**: Understand the impact of the professional engineering solutions in societal and environmental contexts, and demonstrate the knowledge of, and need for sustainble development.
8. **Ethics**: Apply ethical principles and commit to professional ethics and responsibilities and norms of the engineering practice.
9. **Individual and team work**: Function effectively as an individual, and as a member or leader in diverse teams, and in multidisciplinary settings.
10. **Communication**: Communicate effectively on complex engineering activities with the engineering community and with society at large, such as, being able to comprehend and write effective reports and design documentation, make effective presentations, and give and receive clear instructions.
11. **Project management and finance**: Demonstrate knowledge and understanding of the engineering and mangement principles and apply these to one's own work, as a member and leader in a team, to manage projects and in multidisciplinary environments.

12. **Life-long learning**: Recognize the need for, and have the preparation and ability to engage in independent and life-long learning in the broadest context of technological change.

STUDENT HELP DESK

Sr.No	Name of the faculty	Activities
1	Dr.R.R.Maggavi	GATE / Preplacement Coaching
		CN Lab In charge
		Students Mentor
		Module Coordinator
		Research Center Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
2	Prof. S. S. Malaj	GATE / Preplacement Coaching
		Adv.Comm. Lab In charge
		Students Mentor
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		NIRF Coordinator
		Conference Coordinator
3	Prof. S. S. Kamate	GATE / Preplacement Coaching
		VLSI Lab In charge
		Students Mentor
		Module Coordinator
		IEEE Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
4	Prof. D. M. Kumbhar	GATE / Preplacement Coaching
		AC Lab In charge
		Students Mentor
		Dept. Association Coordinator
		Class Teacher
		IIIC Coordinator
		Dept. NAAC Criteria Sub Coordinator
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Dept. ED Cell Coordinator

Sr.No	Name of the faculty	Activities
5	Prof. S. S. Patil	GATE / Preplacement Coaching
		ARM & ES Lab In charge
		Students Mentor
		Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator
		Admission Coordinator
		Module Coordinator
6	Prof. D. B. Madihalli	GATE / Preplacement Coaching
		DSD Lab In charge
		Students Mentor
		NBA Coordinator
		News & Publicity Coordinator
		NBA Criteria Coordinator
		Website Coordinator
		VTU LIC Coordinator
7	Prof. P. V. Patil	GATE / Preplacement Coaching
		HDL Lab In charge
		Students Mentor
		NBA Criteria Coordinator
		T&P Cell Coordinator
		Alumni Coordinator
		Project Coordinator
8	Dr. S. S. Ittannavar	GATE / Preplacement Coaching
		DSP Lab In charge
		Students Mentor
		EMS/ IA Coordinator
		News Letter / Technical Magazine
		AICTE Coordinator
9	Prof. B. P. Khot	GATE / Preplacement Coaching
		MC Lab In charge
		Students Mentor
		Dept. Time Table Coordinator & Meeting Coordinator
		Class Teacher
		NBA Criteria Coordinator
		AICTE Activity Coordinator

CONTENTS

FACULTY POSITION

S.N.	Category	No. in position	Average experience
1	Teaching faculty.	09	16.76Y
2	Technical supporting staff.	04	22.02Y
3	Helper staff	02	21.50Y

MAJOR LABORATORIES

S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs	S. N.	Name of the laboratory	Area in Sq. Mtrs	Amount Invested in Lakhs
1	Digital Electronics Lab	71	1.54	5	VLSI Lab	71	35.51
2	Analog Electronics (ED &I) Lab	92	8.24	6	Project Lab	95	--
3	Advanced Commn & Commn + LIC Lab	92	20.50	7	Research/E-Yantra/DSP & C.N.Lab	71	16.49
4	HDL/MC / EMD Lab	71	19.57	8	Power Electronics Lab	--	4.86
Total Investment In The Department						**Rs. 95.31 Lacs**	

FACULTY DETAILS

TEACHING FACULTY

S.N.	Name and Designation	Qualification	Specialization	Professional Membership	Teaching Exp.	Contact No.
1	Dr. R. R. Maggavi	Ph.D	E&C	LMISTE	18Y.05M	9480275583
2	Smt. S. S. Malaj	M.E.	E & TC	LMISTE	25Y.07M	9731795803
3	Smt.S.S.Kamate	M.Tech	Digital Electronics	LMISTE	20Y.00M	9008696825
4	Sri. D.M. Kumbhar	M.Tech	Electronics	LMISTE	18Y.10M	09373609880
5	Sri. Sachin .S. Patil	M.Tech	VLSI & Embedded	LMISTE	18Y.08M	9448102010
6	Sri .D.B. Madihalli	M.Tech	Industrial Electronics	LMISTE	15Y.07M	9902854324
7	Sri.P.V.Patil	M.Tech	VLSI & Embedded	LMISTE	10Y.04M	9731104059
8	Dr.S .S .Ittannavar	Ph.D	DSP	LMISTE	9Y.11M	9964299498
9	Smt. B. P. Khot	M.Tech	Microelectronics & Control Systems	LMISTE	6Y.11M	9964019501

TECHNICAL SUPPORTING STAFF

S.N.	Name	Qualification	Experience (in years)
1.	Sri. P. S. Desai	DEC	22Y-.07M
2.	Sri. V. V. Guruwodeyar	DEC	31Y-02 M
3.	Sri.M.A.Attar	DEC	12Y-09M

VISVESVARAYA TECHNOLOGICAL UNIVERSITY, BELAGAVI
Scheme of Teaching and Examination 2018 – 19
Outcome Based Education(OBE) and Choice Based Credit System (CBCS)(Effective from the academic year 2018 – 19)

VII SEMESTER

Sl.No	Course and Course code		Course Title	Teaching Department	Teaching Hours /Week			Examination				Credits
					Theory Lecture	Tutorial	Practical/ Drawing	Duration in hours	CIE Marks	SEE Marks	Total Marks	
					L	T	P					
1	PCC	18EC71	Computer Networks		3	--	--	03	40	60	100	3
2	PCC	18EC72	VLSI Design		3	--	--	03	40	60	100	3
3	PEC	18XX73X	Professional Elective - 2		3	--	--	03	40	60	100	3
4	PEC	18XX74X	Professional Elective - 3		3	--	--	03	40	60	100	3
5	OEC	18XX75X	Open Elective -B		3	--	--	03	40	60	100	3
6	PCC	18ECL76	Computer Networks Lab		--	2	2	03	40	60	100	2
7	PCC	18ECL77	VLSI Laboratory		--	2	2	03	40	60	100	2
8	Project	18ECP78	Project Work Phase - 1		--	--	2	--	100	--	100	1
9	Internship	--	Internship	(If not completed during the vacation of VI and VII semesters, it shall be carried out during the vacation of VII and VIII semesters)								
				TOTAL	**15**	4	**6**	**21**	**380**	**420**	**800**	**20**

Note: PCC: Professional core, PEC: Professional Elective.

Professional Elective - 2

Course code under 18XX73X	Course Title
18EC731	Real Time System
18EC732	Satellite Communication
18EC733	Digital Image Processing
18EC734	Data Structures using C++
18EC735	DSP Algorithms &Architecture

Professional Electives - 3

Course code under 18XX74X	Course Title
18EC741	IOT & Wireless Sensor Networks
18EC742	Automotive Electronics
18EC743	Multimedia Communication
18EC744	Cryptography
18EC745	Machine Learning

Open Elective –B

(i) 18EC751 Communication Theory (ii) 18EC752 Neural Networks

Students can select any one of the open electives offered by other Departments except those that are offered by the parent Department (Please refer to the list of open electives under 18XX75X).

Selection of an open elective shall not be allowed if,

- The candidate has studied the same course during the previous semesters of the programme.
- The syllabus content of open elective is similar to that of the Departmental core courses or professional electives.
- A similar course, under any category, is prescribed in the higher semesters of the programme.

Registration to electives shall be documented under the guidance of Programme Coordinator/ Advisor/Mentor.

Project work:

Based on the ability/abilities of the student/s and recommendations of the mentor, a single discipline or a multidisciplinary project can be assigned to an individual student or to a group having not more than 4 students. In extraordinary cases, like the funded projects requiring students from different disciplines, the project student strength can be 5 or 6.

CIE procedure for Project Work Phase - 1:

(i) Single discipline: The CIE marks shall be awarded by a committee consisting of the Head of the concerned Department and two senior faculty members of the Department, one of whom shall be the Guide.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of the project work phase -1 Report (covering Literature Survey, Problem identification, Objectives and Methodology), project presentation skill and question and answer session in the ratio 50:25:25 .The marks awarded for the Project report shall be the same for all the batch mates.

(ii) Interdisciplinary: Continuous Internal Evaluation shall be group wise at the college level with the participation of all guides of the college. Participation of external guide/s, if any, is desirable.

The CIE marks awarded for the project work phase -1, shall be based on the evaluation of project work phase -1 Report, project presentation skill and question and answer session in the ratio 50:25:25.The marks awarded for the project report shall be the same for all the batch mates.

Internship: All the students admitted to III year of BE/B.Tech shall have to undergo mandatory internship of 4 weeks during the vacation of VI and VII semesters and /or VII and VIII semesters. A University examination shall be conducted during VIII semester and the prescribed credit shall be included in VIII semester. Internship shall be considered as a head of passing and shall be considered for the award of degree. Those, who do not take- up/complete the internship shall be declared fail and shall have to complete during subsequent University examination after satisfying the internship requirements.

CALENDER OF EVENT

S J P N Trust's
Hirasugar Institute of Technology, Nidasoshi.
Inculcating Values, Promoting Prosperity
Approved by AICTE, New Delhi, Permanently Affiliated to VTU, Belagavi
Recognized under 2(f) & 12B of UGC Act, 1956
Accredited at 'A' Grade by NAAC & Programmes Accredited by NBA:CSE & ECE

IQAC
File I-11
2022-23 (Odd)
Rev: 00

CALENDAR OF EVENTS FOR THE ACADEMIC YEAR 2022-23 (Odd)

Date	Events
19-09-2022	Commencement of Classes for VII Semester
24-09-2022	NSS Foundation Day
02-10-2022	Gandhi Jayanthi
10-10-2022	Commencement of Classes for V Semester
24-10-2022 to 30-10-2022	Traffic Week
27-10-2022 to 29-10-2022	First Internal Assessment for VII Semester
31-10-2022	Feedback -I on Teaching-Learning for VII Semester
31-10-2022	National Integration Day
31-10-2022	Commencement of Classes for III Semester
01-11-2022	Kannad Rajyothsava
03-11-2022	Display of 1st Internal Assessment Marks and submission of Feedback-I of VII Semester to office
09-11-2022 to 18-11-2022	Environment Awareness Month
22-11-2022	World's Aids Day
26-11-2022	First Assignment Submission of III Semester (PCC + IPCC)
28-11-2022 to 30-11-2022	Second Internal Assessment for VII Semester & First Internal Assessment for III (PCC + IPCC) /V Semester
01-12-2022	Feedback –II on Teaching-Learning for VII Semester & Feedback – I on Teaching-Learning for III/V Semester
06-12-2022	Display of 2nd Internal Assessment Marks and submission of Feedback-II of VII Semester & Display of 1st Internal Assessment Marks and submission of Feedback-I of III/V Semester to office
10-12-2022	Human Rights Day
10-12-2022	Sports Day
23-12-2022 & 24-12-2022	First Lab Internal Assessment for III Semester (PCC+AEC)
26-12-2022 & 27-12-2022	Lab Internal Assessment for VII Semester
29-12-2022 to 31-12-2022	Third Internal Assessment for VII Semester & Second Internal Assessment for III (PCC + IPCC) /V Semester
31-12-2022	Last working day for VII Semester
02-01-2023	Feedback –II on Teaching-Learning for III/V Semester
05-01-2023	Display of Final IA Marks of VII Semester
05-01-2023	Display of 2nd Internal Assessment Marks and submission of Feedback-II of III/V Semester to office
07-01-2023	Second Assignment Submission of III Semester (PCC + IPCC)
12-01-2023	National Youth Day
15-01-2023	NSS Day
20-01-2023 & 21-01-2023	Lab Internal Assessment for V Semester
23-01-2023 to 25-01-2023	Third Internal Assessment for V Semester
26-01-2023	Republic Day
27-01-2023	Last working day for V Semester
30-01-2023 to 01-02-2023	Second Lab Internal Assessment for III Semester (PCC+IPCC+AEC)
31-01-2023	Display of Final IA Marks of V Semester
06-02-2023 to 08-02-2023	Third Internal Assessment for III Semester (PCC)
11-02-2023	Last working day for III Semester
14-02-2023	Display of Final IA Marks of III Semester

September-2022

S	M	T	W	T	F	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	

October-2022

S	M	T	W	T	F	S
						1
2	3	4	5	6	7	8
9	10	11	12	13	14	15
16	17	18	19	20	21	22
23	24	25	26	27	28	29
30	31					

04- Mahanavami, Ayudhapooja 05- Vijayadashami
24- Naraka Chaturdashi, 26- Balipadyami Deepavalli

Novemner-2022

S	M	T	W	T	F	S
		1	2	3	4	5
6	7	8	9	10	11	12
13	14	15	16	17	18	19
20	21	22	23	24	25	26
27	28	29	30			

01- Kannada Rajyothsava, 11- Kanakadasa Jayanti

December-2022

S	M	T	W	T	F	S
				1	2	3
4	5	6	7	8	9	10
11	12	13	14	15	16	17
18	19	20	21	22	23	24
25	26	27	28	29	30	31

January-2023

S	M	T	W	T	F	S
1	2	3	4	5	6	7
8	9	10	11	12	13	14
15	16	17	18	19	20	21
22	23	24	25	26	27	28
29	30	31				

14-Makara Sankranti, 26- Republic Day

February-2023

S	M	T	W	T	F	S
			1	2	3	4
5	6	7	8	9	10	11
12	13	14	15	16	17	18
19	20	21	22	23	24	25
26	27	28				

18- Mahashivaratri

19/9/22
Dr. B. V. Madiggond
Dean (Academics)

19/9
Dr. S. C. Kamate
Principal

Subject Title	**COMPUTER NETWORKS**		
Subject Code	18EC71	**CIE Marks**	40
Number of Lecture Hrs/ Week	03	**Exam Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03
			CREDITS – 03

FACULTY DETAILS:

Name: Dr. Raghavendra R. Maggavi	**Designation:** Associate Professor	**Experience:16**Yrs
No. of times course taught: 00	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II/IV	Analog communication/Principles of communication systems
02	Electronics & Communication Engineering	III	Digital Electronics

2.0 Course Objectives

1. Understand the layering architecture of OSI reference model and TCP/IP protocol suite.
2. Understand the protocols associated with each layer.
3. Learn the different networking architectures and their representations.
4. Learn the functions and services associated with each layer.

3.0 Course Outcomes

At the end of the course students will be able to:

	Course Outcome	RBT Level	POs
C401.1	Understand the concepts of networking thoroughly	L2	PO1 to PO12
C401.2	Describe various networking architectures	L2	PO1 to PO12
C401.3	Identify the protocols and services of different layers.	L2	PO1 to PO12
C401.4	Distinguish the basic network configurations and standards associated with each network	L2	PO1 to PO12
C401.5	Analyze a simple network and measurement of its parameters.	L2	PO1 to PO12
Total Hours of instruction		**40**	

4.0 Course Content

Module-1	RBT Level
Introduction: Data communication: Components, Data representation, Data flow, Networks:Network criteria, Physical Structures, Network types: LAN, WAN, Switching, The Internet.(1.1,1.2, 1.3(1.3.1to 1.3.4 of Text). **Network Models:** Protocol Layering: Scenarios, Principles, Logical Connections, TCP/IPProtocol Suite: Layered Architecture, Layers in TCP/IP suite, Description of layers, Encapsulationand Decapsulation, Addressing, Multiplexing and Demultiplexing, The OSI Model: OSI VersusTCP/IP. (2.1, 2.2, 2.3 of Text)	L1, L2

Module-2	
Data-Link Layer: Introduction: Nodes and Links, Services, Two Categories of link, Sublayers,Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services: Framing,Flow and Error Control, Data Link Layer Protocols: Simple Protocol, Stop and Wait protocol,Piggybacking. (9.1, 9.2(9.2.1, 9.2.2), 11.1, 11.2of Text) **Media Access Control**: Random Access: ALOHA, CSMA, CSMA/CD, CSMA/CA. (12.1 ofText). **Wired and Wireless LANs:** Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN:Architectural Comparison, Characteristics, Access Control. (13.1, 13.2(13.2.1 to 13.2.5), 15.1 ofText)	L1, L2,L3
Module-3	
Network Layer: Introduction, Network Layer services: Packetizing, Routing and Forwarding,Other services, Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4Addresses: Address Space, Classful Addressing, Classless Addressing, DHCP, Network AddressResolution, Forwarding of IP Packets: Based on destination Address and Label. (18.1, 18.2, 18.4,18.5.1, 18.5.2 of Text) **Network Layer Protocols:** Internet Protocol (IP): Datagram Format, Fragmentation, Options,Security of IPv4 Datagrams. (19.1of Text). **Unicast Routing:** Introduction, Routing Algorithms: Distance Vector Routing, Link StateRouting, Path vector routing. (20.1, 20.2of Text)	L1, L2,L3
Module-4	
Transport Layer: Introduction: Transport Layer Services, Connectionless and Connectionoriented Protocols, Transport Layer Protocols: Simple protocol, Stop and wait protocol, Go-BackN Protocol, Selective repeat protocol. (23.1, 23.2.1, 23.2.2, 23.2.3, 23.2.4 of Text) **Transport-Layer Protocols in the Internet:** User Datagram Protocol: User Datagram, UDP Services, UDP Applications, Transmission ControlProtocol: TCP Services, TCP Features, Segment, Connection, State Transition diagram, Windowsin TCP, Flow control, Error control, TCP congestion control.(24.2, 24.3.1, 24.3.2, 24.3.3, 24.3.4, 24.3.5, 24.3.6, 24.3.7, 24.3.8, 24.3.9 of Text)	L1, L2, L3
Module-5	
Application Layer: Introduction: providing services, Application- layer paradigms, StandardClient –Server Protocols: World wide web, Hyper Text Transfer Protocol, FTP: Two connections,Control Connection, Data Connection, Electronic Mail: Architecture, Wed Based Mail, Telnet:Local versus remote logging.Domain Name system: Name space, DNS in internet, Resolution,DNS Messages, Registrars, DDNS, security of DNS. (25.1, 26.1, 26.2, 26.3, 26.4, 26.6 of Text)	L1, L2

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Computer communication network based projects.
02	Higher	Computer communication networks 1&2	OSI model architecture, algorithms of data link layer programs. Routing algorithms.

6.0 Relevance to Real World

SL.No	Real World Mapping
01	Computer communication network-based components.
02	OSI Model creation for analysis.
03	Development of a software application.

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
01	Tutorial	Topic: Lettering, Line, Methods of dimensioning
02	NPTEL	Programming and Applications

8.0 Books Used and Recommended to Students

Text Books
1.**Forouzan, "Data Communications and Networking" , 5th Edition, McGraw Hill, 2013, ISBN: 1-25-906475-3.**
Reference Books
1. James J Kurose, Keith W Ross, Computer Networks, , Pearson Education. 2. Wayarles Tomasi, Introduction to Data Communication and Networking, Pearson Education. 3. Andrew Tanenbaum, "Computer networks", Prentice Hall. 4. William Stallings, "Data and computer communications", Prentice Hall
Additional Study material & e-Books
1. https://lecturenotes.in/subject/609/computer-communication-network-ccn
2. http://freecomputerbooks.com/networkComputerBooks.html

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1) https://vtu.ac.in 2) http://www.bookspar.com/engineering-vtu 3) http://www.rejinpaul.com/2014/10/vtu-ece-notes-vtu-ece-1st-2nd-3rd-4th-5th-6th-7th-8th-semester-lecture-notes-download-link.htmlhttp://www.vlab.co.in/ 4) https://www.youtube.com/results?search_query=microprocessor

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)

- Class work, Assignment, Technical quiz: 10 Marks.
- Internal Assessment test Average of all three Tests 30marks.

SCHEME OF EXAMINATION:

- The question paper will have ten questions.
- Each full question consists of 20marks**.**
- There will be 2 full questions (with a maximum of four sub questions) from each module.
- Each full question will have sub questions covering all the topics under a module
- The students will have to answer 5 full questions, selecting one full question from each module.

12.0 Course Delivery Plan

Module	Lecture No.	Content of Lecturer	% of Portion
Module- 1 Introduction& Network Models	1	Data communication: Components, Data representation, Data flow	20
	2	Networks:Network criteria, Physical Structures	
	3	Network types: LAN, WAN, Switching, The Internet.	
	4	Protocol Layering: Scenarios, Principles, Logical Connections	
	5	TCP/IPProtocol Suite: Layered Architecture	
	6	Layers in TCP/IP suite, Description of layers	

	7	Encapsulationand Decapsulation, Addressing, Multiplexing and Demultiplexing	
	8	The OSI Model: OSI VersusTCP/IP.	
Module- 2 Data-Link Layer, Media Access Control&Wired and Wireless LANs	9	Introduction: Nodes and Links, Services, Two Categories of link, Sublayers	20
	10	Link Layer addressing: Types of addresses, ARP. Data Link Control (DLC) services	
	11	Framing,Flow and Error Control, Data Link Layer Protocols	
	12	Simple Protocol, Stop and Wait protocol,Piggybacking	
	13	Random Access: ALOHA, CSMA	
	14	CSMA/CD, CSMA/CA	
	15	Ethernet Protocol, Standard Ethernet. Introduction to wireless LAN	
	16	Architectural Comparison, Characteristics, Access Control.	
Module -3 Network Layer, Network Layer Protocols& Unicast Routing	17	Introduction, Network Layer services: Packetizing, Routing and Forwarding,Other services	20
	18	Packet Switching: Datagram Approach, Virtual Circuit Approach, IPV4Addresses	
	19	Address Space, Classful Addressing, Classless Addressing, DHCP	
	20	Forwarding of IP Packets: Based on destination Address and Label.	
	21	Internet Protocol (IP): Datagram Format	
	22	Fragmentation, Options, Security of IPv4 Datagrams	
	23	Introduction, Routing Algorithms: Distance Vector Routing	
	24	Link StateRouting, Path vector routing	
Module -4 Transport Layer, Transport-Layer Protocols in the Internet	25	Introduction: Transport Layer Services	20
	26	Connectionless and Connectionoriented Protocols	
	27	Transport Layer Protocols: Simple protocol, Stop and wait protocol	
	28	Go-BackN Protocol, Selective repeat protocol.	
	29	User Datagram Protocol: User Datagram, UDP Services, UDP Applications	
	30	Transmission ControlProtocol: TCP Services	
	31	TCP Features, Segment, Connection, State Transition diagram	
	32	Windowsin TCP, Flow control, Error control, TCP congestion control.	
Module 5: Application Layer	33	Introduction: providing services, Application- layer paradigms	20
	34	StandardClient –Server Protocols	
	35	World wide web, Hyper Text Transfer Protocol	
	36	FTP: Two connections,Control Connection	
	37	Data Connection, Electronic Mail: Architecture	
	38	Wed Based Mail, Telnet:Local versus remote logging.Domain Name system	
	39	Name space, DNS in internet, Resolution,DNS Messages, Registrars	
	40	DDNS, security of DNS	

13.0 University Result

Examination	FCD	FC	SC	% Passing
2021	0	33	1	100

Prepared by	Checked by		
Dr. R. R. Maggavi	Prof. S. S Patil	HOD	Principal

Subject Title	**VLSI Design**		
Subject Code	18EC72	**IA Marks**	40
Number of Lecture Hrs / Week	03 L	**Exam Marks**	60
Total Number of Lecture Hrs	40	**Exam Hours**	03
FACULTY DETAILS:			
Name: Prof. S S Kamate	**Designation:** Asst. Professor	**Experience:** 20 yrs.	
No. of times course taught: 02	**Specialization:** Digital Electronics		

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	III	Analog Electronic Circuits
02	ECE	III	Digital Electronics

2.0 Course Objectives

1. Impart knowledge of MOS transistor theory and CMOS technologies.
2. Learn the operation principles and analysis of inverter circuits.
3. Design Combinational, sequential and dynamic logic circuits as per the requirements.
4. Infer the operation of Semiconductors Memory circuits.
5. Demonstrate the concepts of CMOS testing.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to draw and analyze.

	Course Outcome	Cognitive Level	POs
C402.1	Demonstrate understanding of MOS transistor theory, CMOS fabrication flow and technology scaling.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.2	Draw the basic gates using the stick and layout diagrams with the knowledge of physical design aspects.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.3	Demonstrate ability to design Combinational, sequential and dynamic logic circuits as per the requirements	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.4	Interpret Memory elements along with timing considerations.	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
C402.5	Interpret testing and testability issues in VLSI Design	U	PO1, PO2 PO3, PO5, PO8,PO9, PO10 PO12
Total Hours of instruction		**40**	

4.0 Course Content

Course Content:

Module	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1: **Introduction:** A Brief History, MOS Transistors, CMOS Logic **(1.1 to 1.4 of TEXT2)** **MOS Transistor Theory:** Introduction, Long-channel I-V Characteristics, Non-ideal I-V Effects, DC Transfer Characteristics **(2.1, 2.2, 2.4 and 2.5 of TEXT2).**	**08 Hours**	**L1, L2**
Module 2: **Fabrication:** CMOS Fabrication and Layout, VLSI Design Flow, Introduction, CMOS Technologies, Layout Design Rules, **(1.5 and 3.1 to 3.3 of TEXT2).** MOSFET Scaling and Small-Geometry Effects, MOSFET Capacitances **(3.5 to 3.6 of TEXT1)**	**08 Hours**	**L1, L2**
Module 3: **Delay:** Introduction, Transient Response, RC Delay Model, Linear Delay Model, Logical Efforts of Paths **(4.1 to 4.5 of TEXT2, except sub-sections 4.3.7, 4.4.5, 4.4.6, 4.5.5 and 4.5.6).** **Combinational Circuit Design:** Introduction, Circuit families **(9.1 to 9.2 of TEXT2, except subsection 9.2.4).**	**08 Hours**	**L1, L2, L3**
Module 4: **Sequential Circuit Design:** Introduction, Circuit Design for Latches and Flip-Flops **(10.1 and 10.3.1 to 10.3.4 of TEXT2)** **Dynamic Logic Circuits:** Introduction, Basic Principles of Pass Transistor Circuits, Synchronous Dynamic Circuit Techniques, Dynamic CMOS Circuit Techniques **(9.1, 9.2, 9.4 to 9.5 of TEXT1)**	**08 Hours**	**L1, L2, L3**
Module 5: **Semiconductor Memories:** Introduction, Dynamic Random Access Memory (DRAM) and Static Random Access Memory (SRAM), **(10.1 to 10.3 of TEXT1)** **Testing and Verification:** Introduction, Logic Verification Principles, Manufacturing Test Principles, Design for testability **(15.1, 15.3, 15.5 15.6.1 to 15.6.3 of TEXT 2).**	**08 Hours**	**L1, L2**

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VII	VLSI Lab	VLSI Design of Circuits
02	VIII	Projects on VLSI	Projects and Research

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Analyze different types of VLSI Designs
02	Design of different types of VLSI chips

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: VLSI Lab
02	NPTEL	Demonstration and Application

8.0 Books Used and Recommended to Students

Text Books
1. "CMOS Digital Integrated Circuits: Analysis and Design" - **Sung Mo Kang & Yosuf Leblebici,** Third Edition, Tata McGraw-Hill. **2. "CMOS VLSI Design- A Circuits and Systems Perspective"-** Neil H. E. Weste, and David Money Harris4th Edition, Pearson Education.
Reference Books
1. Adel Sedra and K. C. Smith, "Microelectronics Circuits Theory and Applications", 6th or 7th Edition, Oxford University Press, International Version, 2009. 2. Douglas A Pucknell & Kamran Eshragian, "Basic VLSI Design", PHI 3rd Edition, (original Edition – 1994). 3. Behzad Razavi, "Design of Analog CMOS Integrated Circuits", TMH, 2007.
Additional Study material & e-Books
3. VTU on line notes.

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
01) https://nptel.co.in 02) http://m.noteboy.in/vtuflies 03) https://www.edx.org/school/iitbombayx?utm_source=bing&utm_medium=cpc&utm_term=iit-bombay&utm_campaign=partner-iit-bombay

10.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	IEEE Xplorer	http://ieee.com
2	International Journal of Science and Technology	http://www.sciencedirect.com/science/journal/00207683
3	Journal of Communication Engineering	http://ieee.com

11.0 Examination Note

Internal Assessment: 40 Marks
Three IA will be conducted and average of best of two will be accounted.

Scheme of Evaluation for Internal Assessment (40 Marks)
(a) Internal Assessment test in the same pattern as of the main examination. (50 marks.)

SCHEME OF EXAMINATION:
Two questions to be set from the syllabus covered.
Student has to answer one part from each question.
Question 1 or 2 1x25 = 25Marks
Question 3 or 4 1x25 = 25Marks
Total = 50Marks reduced to 30 Marks
Total CIE marks = 30 from IA + 10 from Assignment or quiz.

INSTRUCTION FOR VLSI Design (18EC72) EXAMINATION
1. Four full questions will be given which consists of a,b,c,d sub sections.
2. Students have to answer either Q :1 or 2 and Q: 3 or 4 completely.

12.0 Course Delivery Plan

Course Delivery Plan:

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Introduction: A Brief History of MOS transistors	20
	2	MOS Transistors	
	3	CMOS Logic	
	4	Introduction MOS Transistor Theory	
	5	Long-channel I-V Characteristics	
	6	Non-ideal I -V Effects	
	7	DC Transfer Characteristics	
	8	Cont'd…	
2	9	Introduction to CMOS Fabrication	
	10	Introduction to CMOS Fabrication and Layout	
	11	Cont'd…	
	12	Cont'd…	
	13	VLSI Design Flow	
	14	Introduction CMOS Technologies	
	15	Layout Design Rules	
	16	MOSFET Scaling	
	17	Small-Geometry Effects	
	18	MOSFET Capacitances	
3	19	Introduction to Transient Response	60
	20	RC Delay Model	
	23	Linear Delay Model	
	24	Logical Efforts of Paths	
	25	Introduction to Combinational Circuit Design Circuit families	
	26	Cont'd…	
	27	Circuit families	
4	28	Introduction to Sequential Circuit Design	80
	29	Circuit Design for Latches	
	30	Circuit Design and Flip-Flops	
	31	Cont'd…	
	32	Introduction to Dynamic Logic Circuits	
	33	Cont'd…	
	34	Basic Principles of Pass Transistor Circuits	
	35	Cont'd…	
5	36	Introduction to Semiconductor Memories	100
	37	Introduction to Dynamic Random Access Memory (DRAM) and	
	38	Cont'd…	
	39	Static Random Access Memory (SRAM)	
	40	Introduction to Testing and Verification	
	41	Logic Verification Principles	
	42	Manufacturing Test Principles	
	43	Design for testability	
	44	Cont'd…	

13.0 QUESTION BANK

MODULE -1

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1. What is Moore's first law? Discuss about evaluation of integrated circuit technology.
2. Compare between different families with respect to speed and power.
3. Draw & explain basic n-MOS enhancement mode transistor action.
4. Draw & explain basic n-MOS depletion mode transistor action.
5. Draw & explain basic p-MOS enhancement mode transistor action.
6. Explain CMOS logic.
7. Explain Long-channel I-V Characteristics.
8. Explain Non-ideal I-V Effects.
9. Explain DC Transfer characteristics

MODULE -2

1. Explain in detail n-MOS fabrication process.
2. Explain in detail p well-CMOS fabrication process.
3. Explain in detail n well-CMOS fabrication process.
4. Explain VLSI design flow.
5. Draw scaled n-MOS transistor for combined voltage & dimension model.
6. Find out scaling factors for all parameters given below –
   gate area (Ag), gate capacitance per unit area (Co), gate capacitance (Cg), parasitic capacitance (Cx), carrier density in channel (Qon), channel resistance (Ron), gate delay (Td), maximum operating frequency (fo), saturation current (Idss), current density (J), switching energy per gate (Eg), power dissipation per gate (Pg), power dissipation per unit area (Pa), speed power product (PT).
8. Find out scaling effect on each factor in each model that is combined voltage & dimensional model, constant field model & constant voltage model in tabular form

MODULE -3

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1. What is transient response?
2. Explain transient response of an inverter.
3. Explain RC delay model
4. Explain Linear delay model.
5. Write a note on logical efforts and paths.
6. Explain combinational logic design.
7. Write a note on combinational logic families.

MODULE -4

1. What sequential circuit design.
2. Write a note on sequential circuit design.
3. Explain circuit design for latches.
4. Explain circuit design for flip-flops.
5. What is a pass transistor?
6. Explain basic principles of pass transistor logic.
7. Explain synchronous dynamic circuit techniques.
8. Explain dynamic circuit techniques.

MODULE-5

1. What are the different timing considerations?
2. Depending upon area requirement, power dissipation & volatility, discuss following memory elements –
   i) Dynamic shift register cell ii) a 3- Transistor dynamic RAM cell iii) a I-transistor dynamic memory cell.

3. Draw & explain a pseudo static RAM cell.
5. Draw circuit diagram of 4-transistor dynamic shift register cell & explain read and write operation with sense amplifier.
6. Draw sense amplifier used in memory array, what it's required?
7. Draw circuit & stick diagram for 6-transistor static CMOS memory cell & explain read *I* write operation with sense amplifier.
8. Give a logical arrangement to implement JK-FF.
9. Explain how D-FF is formed?
10. Explain how *you* will design 4X4 bit register array by using pseudo static memory cell?
11. How you will develop selection & control logic *for* 4X4 bit register array?
12. What is testing?
13. Explain logic Verification Principles
14. Explain Manufacturing Test Principles.
15. Write a note on Design for testability.

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15.0 University Result

Examination	FCD	FC	SC	% Passing
Feb 2022	3	09	23	100

Prepared by	Checked by		
Prof. S.S.Kamate	Prof. S.S .Patil	HOD	Principal

Subject Title	**DIGITAL IMAGE PROCESSING**		
Subject Code	**18EC733**	**IA Marks**	**40**
Number of Lecture Hrs / Week	**03**	**Exam Marks**	**60**
Total Number of Lecture Hrs	**40**	**Exam Hours**	**03**

Faculty Details:		
Name: Prof. B. P. Khot	**Designation: Assistant Professor**	**Experience: 6.8 Years**
No. of times course taught: 06	**Specialization: Microelectronics and control systems**	

1.0 Prerequisite Subjects:

Sr. No.	Branch	Semester	Subject
01	Electronics & Communication	III	Digital Electronics
02	Electronics & Communication	V	Digital signal Processing

2.0 Course Objectives

1. Understand the fundamentals of digital image processing.
2. Understand the image transform used in digital image processing.
3. Understand the image enhancement techniques used in digital image processing.
4. Understand the image restoration techniques and methods used in digital image processing.
5. Understand the Morphological Operations used in digital image processing.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	RBT Level	POs
C403B.1	Understand image formation and the role human visual system plays in perception of gray and color image data.	L1, L2	PO1-PO6, PO10-PO12
C403B.2	Apply image processing techniques in spatial domain.	L1, L2	PO1-PO6, PO10-PO12
C403B.3	Apply image processing techniques in frequency domain	L1, L2	PO1-PO6, PO10-PO12
C403B.4	Conduct independent study and analysis of Image Enhancement and restoration techniques.	L1, L2	PO1-PO6, PO10-PO12
C403B.5	Design and evaluate image analysis techniques	L1, L2	PO1-PO6, PO10-PO12
Total Hours of instruction		40	

4.0 Course Content

Module-1	RBT Level
Digital Image Fundamentals: What is Digital Image Processing?, Origins of Digital Image Processing, Examples of fields that use DIP, Fundamental Steps in Digital Image Processing, Components of an Image Processing System, Elements of Visual Perception, Image Sensing and Acquisition. [Text: Chapter 1 and Chapter 2: Sections 2.1 to 2.2, 2.6.2] 10Hours	L1, L2
Module-2	
Image Enhancement in the Spatial Domain: Image Sampling and Quantization, Some Basic Relationships Between Pixels, Linear and Nonlinear Operations. Some Basic Intensity Transformation Functions, Histogram Processing, Fundamentals of Spatial Filtering, Smoothing Spatial Filters, Sharpening Spatial Filters. [Text:Chapter2:Sections 2.3 to 2.62,Chapter 3:Sections 3.2 to 3.6] 10 Hours	L1, L2
Module-3	
Frequency Domain: Preliminary Concepts, The Discrete Fourier Transform (DFT) of Two Variables, Properties of the 2-D DFT, Filtering in the Frequency Domain, Image Smoothing and Image Sharpening Using Frequency Domain Filters, Selective Filtering. Constrained Least Squares Filtering. [Text: Chapter 4: Sections 4.2, 4.5 to 4.10] 10 Hours	L1, L2
Module-4	
Restoration: Noise models, Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering, Linear, Position Invariant degradations, Estimating the Degradation Function, Inverse Filtering, Minimum Mean Square Error (Wiener) Filtering, Constrained Least Squares Filtering. [Text: Chapter 5: Sections 5.2, to 5.9] 10 Hours	L1, L2
Module-5	
Morphological Image Processing: Preliminaries, Erosion and Dilation, Opening and Closing. **Color Image Processing:** Color Fundamentals, Color Models, Pseudo color Image Processing. [Text: Chapter 6: Sections 6.1 to 6.3, Chapter 9: Sections 9.1 to 9.3] 10 Hours	L1, L2

5.0 Relevance to future subjects

Sr. No.	Semester	Subject	Topics
01	VIII	Project work	Image Processing Projects

6.0 Relevance to Real World

Sr. No.	Real World Mapping
01	Machine vision (Robotics)
02	Medical image Processing
03	Video processing (TVs, monitors, displays)

7.0 Gap Analysis and Mitigation

Sr. No.	Delivery Type	Details
01	Tutorial	Topic: Image Transforms
02	NPTEL	Image Enhancement, Image Restoration

8.0 Books Used and Recommended to Students

Text Books
1. "Digital Image Processing", Rafel C Gonzalez and Richard E. Woods, PHI 3rd Edition 2010.
Reference Books
1. "Digital Image Processing"- S.Jayaraman, S.Esakkirajan, T.Veerakumar, Tata McGraw Hill 2014.
2. "Fundamentals of Digital Image Processing" A. K. Jain, Pearson 2004.
3. Image processing analysis and Machine vision with Mind Tap by Milan Sonka and Roger Boile, Cengage Publications, 2018.

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
1. http://www.nptelvideos.in/2012/12/digital-image-processing.html 2. http://nptel.ac.in/courses/106105032/ 3. http://vtu.allsyllabus.com/ECE/sem_7/Digital_Image_Processing/index.php

10.0 Magazines/Journals Used and Recommended to Students

Sr. No.	Magazines/Journals	Website
1	Introduction of Digital Image Processing	http://textofvideo.nptel.ac.in/117105135/lec1.pdf
2	Digital image fundamentals	http://www.acfr.usyd.edu.au/courses/amme4710/Lectures/AMME4710-Chap2-DigitalImageFundamentals.pdf
3	Image enhancement	https://link.springer.com/content/pdf/10.1007%2F978-1-4471-2751-2_4.pdf
4	Image Enhancement	http://textofvideo.nptel.ac.in/117105079/lec17.pdf
5	Image Restoration - I	http://textofvideo.nptel.ac.in/117105079/lec22.pdf
6	Color Image Processing	http://textofvideo.nptel.ac.in/117105079/lec26.pdf
7	Fundamental Concepts & an Overview of the Wavelet Theory	http://web.iitd.ac.in/~sumeet/WaveletTutorial.pdf
8	Mathematical Morphology- III	http://textofvideo.nptel.ac.in/117105079/lec35.pdf
9	Image Segmentation	http://textofvideo.nptel.ac.in/117105079/lec29.pdf

11.0 Examination Note

Internal Assessment: 40 Marks (IA Marks (30 Marks) + Assignments (10 Marks))

Three IA will be conducted for 50 marks and average of three will be accounted and that will be reduced to 30 marks.

SCHEME OF IA EXAMINATION:

Two questions to be set from the syllabus covered.
Student has to answer one part each from each question.
Question 1 1x25 = 25Marks
Question 2 1x25 = 25Marks
Average of three IA will be accounted and reduced to 30 marks.
Total IA MARKS = 30 Marks

Assignments (10 Marks)

Assignments for each module are to be submitted and evaluated for 25 marks for each. Average of five modules is to be accounted and reduced to 10 marks.

INSTRUCTION FOR DIGITAL IMAGE PROCESSING (18EC733) EXAMINATION:

(a) Examination will be conducted for 100 marks with question paper containing 10 full questions, each of 20 marks.
(b) Each full question can have a maximum of 4 sub questions.
(c) There will be 2 full questions from each module covering all the topics of the module.
(d) Students will have to answer 5 full questions, selecting one full question from each module.

12.0 Course Delivery Plan

MODULE	LECTURE NO.	CONTENT OF LECTURE	% OF PORTION
1	1	Digital Image Fundamentals	20
	2	What is Digital Image Processing?	
	3	Origins of Digital Image Processing	
	4	Examples of fields that use DIP	
	5	Fundamental Steps in Digital Image Processing	
	6	Components of an Image Processing System.	
	7	Elements of Visual Perception.	
	8	Image Sensing and Acquisition.	
2	9	**Image Enhancement in the Spatial Domain**: Image Sampling and Quantization	20
	10	Some Basic Relationships Between Pixels, Linear and Nonlinear Operations	
	11	Some Basic Intensity Transformation Functions	
	12	Histogram Processing	
	13	Fundamentals of Spatial Filtering	
	14	Smoothing Spatial Filters	
	15	Image Smoothing Using Frequency Domain Filters	
	16	Sharpening Spatial Filters	
3	17	**Frequency Domain:** Preliminary Concepts	20
	18	Discrete Fourier Transform (DFT) of Two Variables	
	19	Image Smoothing	
	20	Properties of the 2-D DFT	
	21	Filtering in the Frequency Domain	
	22	Image Sharpening Using Frequency Domain Filters	
	23	Selective Filtering	
	24	Constrained Least Squares Filtering.	

4	25	Restoration: Noise models	20
	26	Restoration in the Presence of Noise Only using Spatial Filtering and Frequency Domain Filtering	
	27	Restoration in the Presence of Noise Only using Frequency Domain Filtering	
	28	Linear, Position Invariant degradations	
	29	Estimating the Degradation Function	
	30	Inverse Filtering	
	31	Minimum Mean Square Error (Wiener) Filtering,	
	32	Constrained Least Squares Filtering.	
5	33	Morphological Image Processing	20
	34	Preliminaries	
	35	Erosion and Dilation	
	36	Opening and Closing	
	37	Color Image Processing	
	38	Color Fundamentals,	
	39	Color Models	
	40	Pseudo color Image Processing	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sr. No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions on Band pass signal to equivalent low pass and Line codes.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 of the syllabus	2	Individual Activity. Printed solution expected.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.
2	Assignment 2: University Questions on Detection and Estimation methods.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 of the syllabus	4	Individual Activity. Printed solution expected.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.
3	Assignment 3: University Questions on digital modulation techniques.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 of the syllabus	5	Individual Activity. Printed solution expected.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.
4	Assignment 4: University Questions on ISI, Eye diagrams and equalizers.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 of the syllabus	6	Individual Activity. Printed solution expected.	Text Book 1, Reference book 1 of the reference list. Website of the Reference list.
5	Assignment 5: University Questions on Spread spectrum modulation.	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 of the syllabus	6	Individual Activity. Printed solution expected.	Text Book 1, Reference book 1, 2 of the reference list. Website of the Reference list.

14.0 QUESTION BANK

Module 1: Digital image fundamentals

1. What is digital image processing?
2. Write a note on origins of digital image processing.
3. Explain the fundamental steps in digital image processing.
4. Explain the fields that use DIP.
5. Explain about visual perception
6. Briefly explain the components of an image processing system.
7. Explain image sensing and acquisition.

Module 2: Image Enhancement in the Spatial Domain :

1. Explain image sampling and quantization.
2. Explain some basic relationships between pixels.
3. Write a note on linear and nonlinear operations.
4. Write a note on basic intensity transformation functions.
5. Explain histogram processing.
6. Explain the fundamentals of spatial filtering.
7. Write a note on smoothing spatial filters
8. Write a note on sharpening spatial filters.

Module 3: Frequency Domain

1. Explain preliminary concepts of selective filtering.
2. Explain Discrete Fourier Transform (DFT) of two variables.
3. Explain properties of the 2-D DFT.
4. Explain filtering in the frequency domain.
5. Write a note on image sharpening using frequency domain filters.
6. Write a note on image smoothing using frequency domain filters.

Module 4: Restoration

1. Write a note on restoration process.
2. Explain noise models.
3. Explain restoration in the presence of noise only, using spatial filtering.
4. Write a note on restoration in the presence of noise only, using frequency domain filtering.
5. Write a note on linear degradations.
6. Explain position-invariant degradations.
7. Explain Minimum Mean Square Error (Wiener) filtering.
8. Explain constrained least squares filtering.

Module 5: Morphological Image Processing, Color Image Processing

1. Write a note on color fundamentals.
2. Write a note on color models.
3. Explain pseudo color image processing.
4. Explain multiresolution expansions in wavelet transform.
5. Write a note on erosion and dilation.
6. Write a note on opening and closing in morphological image processing.

15.0 University Result

Examination	FCD	FC	SC	% Passing
Dec.-2013/Jan-2014	37	04	01	100
Dec.-2014/Jan-2015	13	17	07	100
Dec.-2017/Jan-2018	21	10	04	100
Dec -2018/Jan-2019	31	15	09	100
Dec -2019/Jan-2020	28	09	06	100
Dec -2020/Jan-2021	25	10	00	100

2018 Scheme

Examination	S	A	B	C	D	E	% Passing
Feb 2022	9	12	9	2	3	-	100

Prepared by	Checked by		
Prof. B. P. Khot	Dr. R. R. Maggavi	HOD	Principal

Subject Title	**MACHINE LEARNING WITH PYTHON**		
Subject Code	**18EC745**	**CIE Marks**	**40**
Number of Lecture Hrs /	**03**	**SEE Marks**	**60**
Total Number of Lecture Hrs	**40**	**Exam Hours**	**03**
CREDITS – 03			

FACULTY DETAILS:		
Name: Prof. P.V.PATIL	Designation: Asst. Professor	Experience: 10 years
No. of times course taught:02(including Present)	Specialization: Mtech –(VLSI Design & Embedded Systems)	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	ECE	VI	Python Application Programming

2.0 Course Objectives

The course objective is to make students of ECE branch of engineering to understand the fundamentals of Microwaves and Antennas for Communication Engineering Applications.

3.0 Course Outcomes

Having successfully completed this course, the student will be able to

	Course Outcome	RBT Level	PO's
CO404.1	Identify the problems in machine learning.	L1, L2	1,2,3,4,7,10
CO404.2	Select supervised, unsupervised or reinforcement learning for problem solving.	L1, L2	1,2,3,4,6
CO404.3	Apply theory of probability and statistics in machine learning	L1,L2,L3	1,2,3,4
CO404.4	Apply concept learning, ANN, Bayes classifier, k nearest neighbor	L1, L2, L3, L4	1,2,3,4,6
CO404.5	Perform statistical analysis of machine learning techniques.	L1, L2, L3	1,2,3,4,6
Total Hours of instruction		50	

4.0 Course Content

Modules	Teaching Hours	Bloom's Taxonomy (RBT) level
Module 1	10	L1, L2
Introduction: well posed learning problems, designing learning System , perspective and issues in machine learning. **Concept learning:** concept learning task, concept learning as search, find-s algorithm, Version space, candidate elimination algorithm, inductive bias. **Python libraries suitable for machine learning:** numerical analysis and data exploration with Numpy arrays, and data visualization with mat plot lib **Text book1, sections: 1.1 – 1.3, 2.1-2.5, 2.7**		
Module -2	10	L1, L2
Decision Tree Learning: Decision tree representation, Appropriate problems for decision tree learning, Basic decision tree learning algorithm, hypothesis space search in decision tree learning, Inductive bias in decision tree learning, Issues in decision tree learning. Example program in Python **Text Book1, Sections: 3.1-3.7**		

Module-3	08	L1,L2L3
Artificial Neural Networks: Introduction, Neural Network representation, Appropriate problems, Perceptrons, Back propagation algorithm. Example program in Python **Text book 1, Sections: 4.1 – 4.6**		
Module-4	10	L1, L2,L3,L4
Bayesian Learning: Introduction, Bayes theorem, Bayes theorem and concept learning, ML and LS error hypothesis, ML for predicting probabilities, MDL principle, Naive Bayes classifier, Bayesian belief networks, EM algorithm, Example program in Python. **Text book 1, Sections: 6.1 – 6.6, 6.9, 6.11, 6.12**		
Module-5	12	L1, L2,L3
Evaluating Hypothesis: Motivation, Estimating hypothesis accuracy, Basics of sampling theorem, General approach for deriving confidence intervals, Difference in error of two hypothesis, Comparing learning algorithms. **Instance Based Learning:** Introduction, k-nearest neighbor learning, locally weighted regression, radial basis function, cased-based reasoning, **Reinforcement Learning:** Introduction, Learning Task, Q Learning Example program in Python. **Text book 1, Sections: 5.1-5.6, 8.1-8.5, 13.1-13.3**		

5.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Machine Learning

6.0 Books Used and Recommended to Students

Text Books
Tom M. Mitchell, Machine Learning**,** India Edition 2013, McGraw Hill Education.
Reference Books
1. Trevor Hastie, Robert Tibshirani, Jerome Friedman, h The Elements of Statistical Learning, 2nd edition, springer series in statistics. **2. Ethem Alpaydın, Introduction to machine learning, second edition, MIT press.** **3. https://www.analyticsvidhya.com/blog/2015/04/comprehensive-guide-data-exploration-sas-using-pythonnumpy-scipy-matplotlib-pandas/** **4. https://www.oreilly.com/library/view/python-for-data/9781491957653/ch01.html**

7.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
3) *nptel.ac.in* 4) *VTU e-learning notes*

8.0 Magazines/Journals Used and Recommended to Students

Sl. No	Magazines/Journals	website
1	Machine Learning using Python	www.ieee.org

9.0 Examination Note

Scheme of Evaluation for CIE (40 Marks)

Internal Assessment test will be done in the same pattern as that of the main examination.
Internal Assessment: 30 Marks
Assignment: 10 Marks

SCHEME OF EXAMINATION: 100 Marks, scaled down to 60 in VTU result sheet.
The question paper will have ten questions.

- Each full question is for 20 marks.
- There will be 2 full questions (with a maximum of three sub questions in one full question) from each module.
- Each full question with sub questions will cover the contents under a module.
- Students will have to answer 5 full questions, selecting one full question from each module.

10.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	% of Portion
1	1	Well posed learning problems ,	20
	2	Designing learning System	
	3	Perspective and issues in machine learning.	
	4	Concept learning task	
	5	Concept learning as search find-s algorithm	
	6	Version space	
	7	Numerical analysis and data exploration with Numpy arrays	
	8	Data visualization with mat plot lib	
2	11	Decision tree representation	40
	12	Appropriate problems for decision tree learning	
	13	Basic decision tree learning algorithm	
	14	Hpothesis space search in decision tree learning	
	15	Inductive bias in decision tree learning	
	16	Issues in decision tree learning	
	17	Example program in Python	
3	21	Introduction	60
	22	Neural Network representation	
	23	Appropriate problems	
	24	Perceptrons	
	25	Back propagation algorithm	
	26	Example program in Python	
4	31	Introduction	80
	32	Bayes theorem and concept learning	
	33	ML and LS error hypothesis	
	34	ML for predicting probabilities	
	35	MDL principle	
	36	Naive Bayes classifier	
	37	Bayesian belief networks	
	38	EM algorithm	
	39	Example program in Python	

	41	Motivation, Estimating hypothesis accuracy	
	42	Basics of sampling theorem	
	43	General approach for deriving confidence intervals	

5	44	Difference in error of two hypothesis	100
	45	Comparing learning algorithms.	
	46	Lnstance Based Learning: Introduction	
	47	K-nearest neighbor learning	
	48	Locally weighted regression	
	49	Cased-based reasoning	
	50	Numerical Problems	
	51	Reinforcement Learning: Introduction	
	52	Learning Task	
	53	Q Learning Example program in Python	

11.0 QUESTION BANK

Module – 1

1. Explain the Well posed learning problems.
2. Explain Designing learning System
3. Explain Perspective and issues in machine learning.
4. Explain the Concept learning task
5. Explain the Version space
6. Explain Numerical analysis and data exploration with Numpy arrays
7. Explain Data visualization with mat plot lib

Module-2

1. Explain the Decision tree representation.
2. What are Appropriate problems for decision tree learning
3. Explain the Basic decision tree learning algorithm
4. Explain Hpothesis space search in decision tree learning
5. Explain Inductive bias in decision tree learning
6. Explain Issues in decision tree learning

Module-3

1. Explain the Neural Network representation.
2. Explain Perceptrons
3. Explain Back propagation algorithm.
4. Explain program in Python.

Module-4

1. Explain the Bayes theorem and concept learning.
2. Explain ML and LS error hypothesis
3. Explain ML for predicting probabilities
4. Explain program in Python.
5. Explain MDL principle
6. Explain the Naive Bayes classifier
7. Explain the Bayesian belief networks
8. Explain the EM algorithm

Module-5

1. Explain the Motivation, Estimating hypothesis accuracy.
2. Explain Basics of sampling theorem
3. Explain General approach for deriving confidence intervals
4. Explain Difference in error of two hypothesis
5. Explain Comparing learning algorithms.

6. Explain the Lnstance Based Learning
7. Explain the K-nearest neighbor learning
8. Explain the Locally weighted regression
9. Explain the Cased-based reasoning
10. Explain the Reinforcement Learning.
11. Explain the Learning Task.
12. Explain the Q Learning .

12.0 University Result

Examination	Total	S+	FCD	FC	SC	% Passing
2021-22	35	5	5	16	9	100

Prepared by	Checked by		
Prof. P.V.PATIL	Dr. R. R. Maggavi	HOD	Principal

Subject Title	**ENERGY AND ENVIRONMENT**		
Subject Code	18ME751	**IA Marks**	40
No of Lecture Hrs + Tutorial Hrs / Week	03	**Exam Marks**	60
Total No of Lecture + Tutorial Hrs	40	**Exam Hours**	03
			CREDITS – 03

FACULTY DETAILS:		
Name: Dr. M. M. Shivashimpi	**Designation:** Associate Professor	**Experience:** 15 Years
No. of times course taught: 01	**Specialization:** Thermal Power Engineering	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
1	Common to all	I/II	Chemistry
2	Common to all	I/II	Physics
3	Common to all	V	Environmental Studies

2.0 Course Objectives

1. To understand the fundamentals of energy sources, energy use, energy efficiency, and resulting environmental implications of various energy supplies.
2. To learn about methods of energy storage, energy management and economic analysis
3. To understand the causes and remedies related to social issues like global warming, ozone layer depletion, climate change etc.
4. To understand environment and its ecosystems.
5. To introduce various aspects of environmental pollution and its control. To introduce various acts related to prevention and control of pollution of water and air, forest protection act, wild life protection act etc.

3.0 Course Outcomes

The student, after successful completion of the course, will be able to

CO	Course Outcome	RBT level	POs
CO1	Summarize the basic concepts of energy, its distribution and general Scenario.	L1	PO1, PO6, PO7, PO8, PO9, PO10, PO11, PO12
CO2	Explain different energy storage systems, energy management, audit and economic analysis.	L2	PO1, PO2, PO3, PO6, PO7, PO8, PO9, PO10, PO11, PO12
CO3	Summarize the environment eco system and its need for awareness.	L1	PO1, PO6, PO7, PO8, PO10, PO12
C04	Identify the various types of environment pollution and their effects.	L1	PO1, PO6, PO7, PO8, PO10, PO12
C05	Discuss the social issues of the environment with associated acts.	L2	PO1, PO6, PO7, PO8, PO10, PO12
Total Hours of instruction		**40**	

4.0 Course Content

Module-1: Basic Introduction to Energy: Energy and power, forms of energy, primary energy sources, energy flows, world energy production and consumption, Key energy trends in India: Demand, Electricity, Access to modern energy, Energy production and trade, Factors affecting India's energy development: Economy and demographics Policy and institutional framework, Energy prices and affordability, Social and environmental aspects, Investment. (8 Hours)

Module-2: Energy storage systems: Thermal energy storage methods, Energy saving, Thermal energy storage systems Energy Management: Principles of Energy Management, Energy demand estimation, Energy pricing Energy Audit: Purpose, Methodology with respect to process Industries, Characteristic method employed in Certain Energy Intensive Industries. (8 Hours)

Module-3: Environment: Introduction, Multidisciplinary nature of environmental studies- Definition, scope and importance, Need for public awareness. Ecosystem: Concept, Energy flow, Structure and function of an ecosystem. Food chains, food webs and ecological pyramids, Forest ecosystem, Grassland ecosystem, Desert ecosystem and Aquatic ecosystems, Ecological succession.

Module-4: Environmental Pollution: Definition, Cause, effects and control measures of - Air pollution, Water pollution, Soil pollution, Marine pollution, Noise pollution, Thermal pollution and Nuclear hazards, Solid waste Management, Disaster management Role of an individual in prevention of pollution, Pollution case studies. (8 Hours)

Module-5: Social Issues and the Environment: Climate change, global warming, acid rain, ozone layer depletion, nuclear accidents and holocaust. Case Studies. Wasteland reclamation, Consumerism and waste products, Environment Protection Act, Air (Prevention and Control of Pollution) Act, Water (Prevention and control of Pollution) Act, Wildlife Protection Act, Forest Conservation Act, Issues involved in enforcement of environmental legislation. Group assignments: Assignments related to e-waste management; Municipal solid waste management; Air pollution control systems; Water treatment systems; Wastewater treatment plants; Solar heating systems; Solar power plants; Thermal power plants; Hydroelectric power plants; Bio-fuels; Environmental status assessments; Energy status assessments etc. (8 Hours)

5.0 Relevance to future subjects/Career

SL. No	Semester	Subject	Topics / Relevance
01	VII & VIII	Project Phase-1 & Pahse-2	All modules
02	After graduation	Energy and Pollution Analysis and resolving related problems	All modules

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Electrical Engineering and Automobile Engineering
02	Power plant engineering, thermal power plant
03	Environmental Science

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	nptel.ac.in	E- Learning
02	VTU, E- learning	E- Learning
03	Open courseware	E- Learning

8.0 Books Used and Recommended to Students

Text Books
1. Textbook for Environmental Studies For Undergraduate Courses of all Branches of Higher Education by University grant commission and Bharathi Vidyapeeth Institute of environment education and Research ,Pune 2. De, B. K., Energy Management audit & Conservation, 2nd Edition, Vrinda Publication, 2010.
Reference Books
1. Turner, W. C., Doty, S. and Truner, W. C., Energy Management Hand book, 7th edition, Fairmont Press, 2009. 2. Murphy, W. R., Energy Management, Elsevier, 2007. 3. Smith, C. B., Energy Management Principles, Pergamum, 2007 4. Environment pollution control Engineering by C S rao, New Age International, 2006, reprint 2015, 2nd edition 5. Environmental studies, by Benny Joseph, Tata McGraw Hill, 2008, 2nd edition.
Additional Study material & e-Books
• Nptel.ac.in • VTU, E- learning • India Energy Outlook 2015(www.iea.org/.../IndiaEnergyOutlook_WEO2015.pdf) • Open courseware

9.0 Relevant Websites (Reputed Universities and Others) for Notes/Animation/Videos Recommended

Website and Internet Contents References
1. http://www.nptel.ac.in 2. www.iea.org

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	Elsevier	https://www.journals.elsevier.com/renewable-energy
2	Environmental Sciences Journals	https://www.omicsonline.org/environmental-sciences-journals

11.0 Examination Note

Internal Assessment: 40 Marks
Theoretical aspects as well as relevant sketches should be drawn neatly for questions asked in Internal Assessments
Scheme of Evaluation for Internal Assessment

Internal Assessment test in the same pattern as that of the main examination (Better of the two Tests):40marks.

SCHEME OF EXAMINATION:

- There are five modules two questions from each module
- Student has to answer any five question choosing at least one questions from each module.

  Max. Marks: 60Marks

12.0 Course Delivery Plan

Module No.	Lecture No.	Content of Lecture	% of Portion
1		**Basic Introduction to Energy:**	20
	1	Energy and power, forms of energy, primary energy sources	
	2	Energy flows, world energy production and consumption	
	4	Key energy trends in India: Demand	
	5	Electricity, Access to modern energy,	
	6	Energy production and trade, Factors affecting India's energy development	
	7	Economy and demographics Policy and institutional framework	
	8	Energy prices and affordability, Social and environmental aspects, Investment	
2		**Energy storage systems, Energy Management, Energy Audit, Economic Analysis**	20
	1	Thermal energy storage methods,	
	2	Energy saving, Thermal energy, storage systems	
	3	Principles of Energy Management,	
	4	Energy demand.	
	5	Energy estimation, Energy pricing	
	6	Energy Audit: Purpose	
	7	Methodology with respect to process Industries,	
	8	Characteristic method employed in Certain Energy Intensive Industries.	
	9	Economic Analysis: Scope	
	10	Characterization of an Investment Project	
3		**Environment, Ecosystem:**	20
	1	Environment**:** Introduction, Multidisciplinary nature of environmental studies**-** Definition, scope and importance.	
	2	Need for public awareness.	
	3	Ecosystem**:** Concept, Energy flow Structure and function of an ecosystem.	
	4	Food chains, food webs and ecological pyramids	
	5	Forest ecosystem, Grassland ecosystem,	
	6	Desert ecosystem and Aquatic ecosystems,	
	7	Desert ecosystem and Aquatic ecosystems	
	8	Ecological succession	
4		**Environmental Pollution:**	20
	1	Environmental Pollution definition, Cause and effects	
	2	Control measures of - Air pollution,	
	3	Water pollution, Soil pollution,	
	4	Marine pollution, Noise pollution.	
	5	Thermal pollution and Nuclear hazards ,	
	6	Solid waste Management, Disaster management	
	7	Role of an individual in prevention of pollution	
	8	Pollution case studies	
5		**Social Issues and the Environment:**	20
	1	Climate change, global warming, acid rain, ozone layer depletion	
	2	Nuclear accidents and holocaust. Case Studies.	
	3	Wasteland reclamation, Consumerism and waste products	
	4	Environment Protection Act	
	5	Air (Prevention and Control of Pollution) Act	
	6	Water (Prevention and control of Pollution) Act, Wildlife Protection Act,	
	7	Forest Conservation Act,	
	8	Issues involved in enforcement of environmental legislation	

13.0 Assignments, Pop Quiz, Mini Project, Seminars

Sl.No.	Title	Outcome expected	Allied study	Week No.	Individual / Group activity	Reference: book/website /Paper
1	Assignment 1: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 1 syllabus	3	Individual Activity and submission of hard copy.	Book 1 and all the reference book
2	Assignment 2: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 2 syllabus	6	Individual Activity and submission of hard copy.	Book 1 and all the reference book
3	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 3 syllabus	9	Individual Activity and submission of hard copy.	Book 1 and all the reference book
4	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 4 syllabus	12	Individual Activity and submission of hard copy.	Book 1 and all the reference book
5	Assignment 3: University Questions	Students study the Topics and write the Answers. Get practice to solve university questions.	Module 5 syllabus	15	Individual Activity and submission of hard copy.	Book 1 and all the reference book

15.0 QUESTION BANK

Sl. No	Questions
Unit-I	1. Interpret World Energy Scenario with respect to production and consumption using relevant statistics 2. Define Energy and Power. Differentiate the same. 3. Outline the factors that affect India's energy development. 4. Explain the various key energy trends in India. 5. With relevant statistics, enumerate the primary energy production trend for India.
Unit-II	1. Explain in the detail the various phases of energy audit methodology. 2. List the various thermal energy storage methods. Explain sensible heat and latent heat storage methods. 3. Define Energy audit. Explain the need for energy audit. 4. Write a short note on energy demand estimation. 5. Calculate the cost of generation per kWh for a power station having the following data: Installed capacity of the plant = 200 MW , Capital cost = Rs 400 crores ,Rate of interest and depreciation = 12% , Annual cost of fuel, salaries and taxation = Rs 5 crores Load factor = 50% Also estimate the saving in cost per kWh if the annual load factor is raisedto 60%. 6. Explain in the detail the various phases of energy audit methodology 7. Elaborate the benefits of thermal energy storage.
Unit-III	1. What is an ecosystem? Discuss forest ecosystem. Explain how conservation of forest can be done. 2. Discuss how oxygen cycle is utilized in the ecosystem. 3. Write a short note on (i) ecological succession (ii) food chain, food web and ecological pyramid. 4. Elaborate how the nitrogen cycle ecosystem operates. 5. Enumerate the utilization of carbon in ecosystem. 6. Describe grassland ecosystem. What are its types? How conservation of grassland can be made 7. Discuss how oxygen cycle is utilized in the ecosystem 8. Define Environment. Mention its scope. Discuss the need for public awareness
Unit-IV	1. Discuss briefly the causes, effects and control measures of air pollution. 2. Discuss Solid Waste Management techniques. 3. Elaborate the causes, effects and control measures of (i) Soil Pollution (ii) Noise Pollution (iii) Thermal Pollution 4. Enumerate the role of an individual in prevention of pollution.

	5. Enumerate the water pollution causes and its effects. Mention the control measures that can be initiated for mitigating the same. 6. Discuss any two case studies related to pollution of environment in detail. 7. Elaborate the causes, effects and control measures of (i) Soil Pollution (ii) Noise Pollution (iii) Thermal Pollution 8. Discuss Solid Waste Management techniques.
Unit-V	1. What is acid rain? What are its effects? 2. Explain the salient features of Air Pollution act. 3. Explain about Environment Impact Assessment (EIA). 4. Discuss (i) Wildlife Protection act (ii) Forest Conservation act 5. Write a note on ozone layer depletion. 6. Express the need for reclaiming the wasteland and its development 7. What are the regulations governing water pollution prevention act? 8. Enumerate the impact of global warming on our mother nature.

16.0 University Result

Year	S,A (FCD)	B (FC)	C,D,E (SC)	%age of passing
February/ March 2022	57	06	00	100

Prepared by	Checked by		
Dr. M. M. Shivashimpi	Dr.K.M. Akkoli	HOD	Principal

Subject Title	**COMPUTER NETWORKS LABORATORY**		
Subject Code	18ECL76	**IA Marks**	40
Number of Lecture Hrs/ Week	2Hr Tutorial + 2 Hrs Lab	**Exam Marks**	60
		Exam Hours	03
CREDITS – 02			

FACULTY DETAILS:		
Name: Prof. B. P. Khot	**Designation: Assistant Professor**	**Experience: 6.8 Years**
No. of times course taught: 01	**Specialization: Microelectronics and control systems**	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	I/II	C-Programming
02	Electronics & Communication Engineering	III	Digital Electronics

2.0 Course Objectives

This course will enable students to:

- Choose suitable tools to model a network and understand the protocols at various OSI reference levels.
- Design a suitable network and simulate using a Network simulator tool.
- Simulate the networking concepts and protocols using C/C++ programming.
- Model the networks for different configurations and analyze the results.

3.0 Course Outcomes

	Course Outcome	RBT Level	POs
C406.1	Choose suitable tools to model network and understand the protocols at various OSI reference levels.	L1,L2, L3	PO1- PO6, PO8, PO10- PO12
C406.2	Design a suitable network and simulate using a network simulator tool.	L1,L2, L3	PO1- PO6, PO8, PO10- PO12
C406.3	Analyze the networking concepts and protocols using C/C++ Programming.	L1,L2,L3	PO1- PO6, PO8, PO10- PO12
C406.4	Model the networks for different configurations and analyze the results.	L1,L2,L3	PO1- PO6, PO8, PO10- PO12
Total Hours of instruction		**36**	

4.0 Course Content

PART-A: Simulation experiments using NS2/ NS3/ OPNET/ NCTUns/ NetSim/ QualNet/ Packet Tracer or any other equivalent tool.

1. Implement a point to pint network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.
2. Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.
3. Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.
4. Implement Ethernet LAN using n nodes and assign multiple-traffic to the nodes and obtain congestion window for different sources/ destinations.
5. Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.
6. Implementation of Link state routing algorithm.

PART-B: Implement the following in C/C++

1. Write a program for a HLDC frame to perform the following.
   i) Bit stuffing
   ii)Character stuffing.
2. Write a program for distance vector algorithm to find suitable path for transmission.
3. Implement Dijkstra's algorithm to compute the shortest routing path.
4. For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the program for the cases
   a. Without-error
   b. With error
5. Implementation of Stop and Wait Protocol and Sliding Window Protocol
6. Write a program for congestion control using leaky bucket algorithm.

5.0 Relevance to future subjects

Sl No	Semester	Subject	Topics
01	VIII	Project work	Projects Based on Computer Networks.
02	VIII	HPCN	Advance Computer Networks.

6.0 Relevance to Real World

SL. No	Real World Mapping
01	Design of networking components like modems, firewalls, routers etc.
02	Model creation for analysis
03	Development of a software application.

7.0 Gap Analysis and Mitigation

Sl. No	Delivery Type	Details
01	Tutorial	Topic: Routing algorithms, understanding simulation software's.
02	NPTEL	C/C++ Programming

8.0 Books Used and Recommended to Students

Text Books

1. Data Communications and Networking, Forouzan, 5th Edition, McGraw Hill,2016 ISBN: 1-25-906475-3.
2. Computer Networks, James J Kurose, Keith W Ross, Pearson Education, 2013, ISBN: 0-273-76896-4
3. Introduction to Data Communication and Networking, Wayarles Tomasi, Pearson Education, 2007, ISBN:0130138282

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References

http://nptel.ac.in/courses/106105081/1 2) http://searchnetworking.techtarget.com/
3) https://in.udacity.com/auth?next=/course/computer-networking--ud436

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	Elsevier	https://www.journals.elsevier.com/computer-networks/
2	Sciencedirect	https://www.sciencedirect.com/science/journal/13891286

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (40 Marks)
(a) Lab work, Assignment, Technical quiz: 10 Marks.
(b) Internal Assessment test at the end of semester: 30 Marks.

SCHEME OF EXAMINATION:
Execute Two questions
Two questions to be set, one from Part-A and one from Part-B
Student has to answer both full questions.
100marks Marks divided in three parts, Write up 15 marks, Conduction 70 marks & Viva 15marks.

12.0 Course Delivery Plan

Expt.	Lecture No.	Content	% of Portion
1	1	Implement a point to pint network with four nodes and duplex links between them. Analyze the network performance by setting the queue size and varying the bandwidth.	8.33
2	2	Implement a four node point to point network with links n0-n2, n1-n2 and n2-n3. Apply TCP agent between n0-n3 and UDP between n1-n3. Apply relevant applications over TCP and UDP agents changing the parameter and determine the number of packets sent by TCP/UDP.	16.66
3	3	Implement Ethernet LAN using n (6-10) nodes. Compare the throughput by changing the error rate and data rate.	25
4	4	Implement Ethernet LAN using n nodes and assign multiple traffic to the nodes and obtain congestion window for different sources/ destinations.	33.33
5	5	Implement ESS with transmission nodes in Wireless LAN and obtain the performance parameters.	41.6
6	6	Implementation of Link state routing algorithm.	50
7	7	Write a program for a HLDC frame to perform the following. i) Bit stuffingii) Character stuffing.	58.33
8	8	Write a program for distance vector algorithm to find suitable path for transmission.	66.66
9	9	Implement Dijkstra's algorithm to compute the shortest routing path.	75
10	10	For the given data, use CRC-CCITT polynomial to obtain CRC code. Verify the Program for the cases a. Without error b. With error	83.33
11	11	Implementation of Stop and Wait Protocol and Sliding Window Protocol.	91.66
12	12	Write a program for congestion control using leaky bucket algorithm.	100

13.0 VIVA QUESTION BANK

1. What are functions of different layers?
2. Differentiate between TCP/IP Layers and OSI Layers
3. Why header is required?
4. What is the use of adding header and trailer to frames?
5. What is encapsulation?
6. Why fragmentation requires?
7. What is MTU?
8. Which layer imposes MTU?
9. Differentiate between flow control and congestion control.
10. Differentiate between Point-to-Point Connection and End-to-End connections.
11. What are protocols running in different layers?
12. What is Protocol Stack?
13. Differentiate between TCP and UDP.
14. Differentiate between Connectionless and connection oriented connection.
15. Why frame sorting is required?

16. What is meant by subnet?
17. What is meant by Gateway?
18. What is an IP address?
19. What is MAC address?
20. Why IP address is required when we have MAC address?
21. What is meant by port?
22. What are ephemerical port number and well known port numbers?
23. What is a socket?
24. What are the parameters of socket()?
25. Describe bind(), listen(), accept(), connect(), send() and recv().
26. What are system calls? Mention few of them.
27. What is IPC? Name three techniques.
28. Explain mkfifo(), open(), close() with parameters.
29. What is meant by file descriptor?
30. What is meant by traffic shaping?
31. How do you classify congestion control algorithms?
32. Differentiate between Leaky bucket and Token bucket.
33. How do you implement Leaky bucket?
34. How do you generate busty traffic?
35. What is the polynomial used in CRC-CCITT?
36. What are the other error detection algorithms?
37. What is difference between CRC and Hamming code?
38. Why Hamming code is called 7,4 code?
39. What is odd parity and even parity?
40. What is meant by syndrome?
41. What is generator matrix?
42. What are Routing algorithms?
43. How do you classify routing algorithms? Give examples for each.
44. What are drawbacks in distance vector algorithm?
45. How routers update distances to each of its neighbor?
46. How do you overcome count to infinity problem?
47. What is cryptography?
48. How do you classify cryptographic algorithms?
49. What is public key?
50. What is private key?
51. What are key cipher text and plaintext?
52. What is simulation?
53. What are advantages of simulation?

14.0 University Result

Examination	S	A	B	C	D	E	% Passing
Feb 2022	17	12	2	1	2	-	**100**

Prepared by	Checked by		
Prof. B. P. Khot	Dr. R. R. Maggavi	HOD	Principal

Subject Title	**VLSI LABORATORY**		
Subject Code	18ECL77	**IA Marks**	40
Number of Lecture Hrs / Week	1 Hr Tutorial + 2 Hrs Lab	**Exam Marks**	100
Total Number of Lecture Hrs	40	**Exam Hours**	03

FACULTY DETAILS:		
Name: Prof. S. S. KAMATE	**Designation:** Asst. Professor	**Experience:** T-20.00Yrs, I-00Yrs
No. of times course taught: 02	**Specialization:** Digital Electronics	

1.0 Prerequisite Subjects:

Sl. No	Branch	Semester	Subject
01	Electronics & Communication Engineering	III	Digital Electronics
02	Electronics & Communication Engineering	V	Fundamentals of CMOS VLSI
03	Electronics & Communication Engineering	VI	Microelectronics Circuits

2.0 Course Objectives

This course will enable students to:
- Design, model, simulate and verify CMOS digital circuits
- Design layouts and perform physical verification of CMOS digital circuits
- Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level netlist
- Perform RTL-GDSII flow and understand the stages in ASIC design.

3.0 Course Outcomes

At the end of the course students will be able to:

	Course Outcome	Cognitive Level	POs
C407.1	Design and simulate combinational and sequential digital circuits using Verilog HDL	U	PO1 to PO12
C407.2	Understand the Synthesis process of digital circuits using EDA tool	U	PO1 to PO12
C407.3	Perform ASIC design flow and understand the process of synthesis, synthesis constraints and evaluating the synthesis reports to obtain optimum gate level net list	U	PO1 to PO12
C407.4	Design and simulate basic CMOS circuits like inverter, common source amplifier and differential amplifiers.	U	PO1 to PO12
C407.5	Perform RTL-GDSII flow and understand the stages in ASIC design	U	PO1 to PO12
Total Hours of instruction		**40**	

4.0 Course Content

Laboratory Experiments

Part – A

Analog Design

Use any VLSI design tools to carry out the experiments, use library files and technology files below 180 nm.

1. a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp, Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following:

a. Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time periodof 20ns and plot the input voltage and output voltage of designed inverter?

b. From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width?
c. Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?

1. b) Draw layout of inverter with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

2. a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results.

2. b)Draw layout of NAND withWp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

3.a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB.

1. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.
4. a)Capture schematic of two-stage operational amplifier and measure the following:
   a. UGB
   b. dB bandwidth
   c. Gain margin and phase margin with and without coupling capacitance
   d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality
   e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations.
4. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations.

Part - B

Digital Design

Carry out the experiments using semicustom design flow or ASIC design flow, use technology library 180/90/45nm and below

Note: The experiments can also be carried out using FPGA design flow, it is required to set appropriate constraints in FPGA advanced synthesis options

1.Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following:
a. Verify the functionality using test bench
b.Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement.
c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.
2.Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.
3.Write verilog code for UART and carry out the following:
a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library and by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
4. Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling.
a. Perform functional verification using test bench
b. Synthesize the design targeting suitable library by setting area and timing constraints
c. For various constrains set, tabulate the area, power and delay for the synthesized netlist
d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints
Compare the synthesis results of ALU modeled using IF and CASE statements.
5. Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).
6. For the synthesized netlist carry out the following for any two above experiments:
a. Floor planning (automatic), identify the placement of pads

b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells c. Physical verification and record the LVS and DRC reports.
d. Perform Back annotation and verify the functionality of the design.
e. Generate GDSII and record the number of masks and its color composition.

5.0 Relevance to future subjects

SL. No	Semester	Subject	Topics
01	VIII	Project work	VLSI based projects
02	Higher	VLSI era	Exposure to the VLSI flow and different types of design.

6.0 Relevance to Real World

SL. No	Real World Mapping
01	VLSI design
02	Miniaturization of different designs to provide more flexibility for the designers

7.0 Gap Analysis and Mitigation

SL. No	Delivery Type	Details
02	NPTEL	VLSI design methods

8.0 Books Used and Recommended to Students

Text Books
1. **"**Basic VLSI Design" by Douglas A. Pucknell and Kamran Eshaghian
2. "CMOS VLSI Design"- A Circuits and Systems Perspective**"**- Neil H.E. Weste, David Harris, Ayan Banerjee, 3rd Edition, Pearson Education.
3. "FPGA Based System Design"-Wayne Wolf, Pearson Education, 2004, Technology and Engineering

9.0 Relevant Websites (Reputed Universities and Others) for Notes /Animation / Videos Recommended

Website and Internet Contents References
2) https://vtu.ac.in
3) http://www.bookspar.com/engineering-vtu
3) http://www.slideshare.net/farohalolya/8086-microprocessor-lab-manual
4) https://www.youtube.com/results?search_query=microprocessor

10.0 Magazines/Journals Used and Recommended to Students

Sl.No	Magazines/Journals	website
1	IEEE	http://ieeexplore.ieee.org/Xplore/home.jsp
2	PC World	http://www.pcworld.com/article/146957/components/article.html

11.0 Examination Note

Scheme of Evaluation for Internal Assessment (20 Marks)
(c) Lab work, Assignment, Technical quiz : 5Marks.
(d) Internal Assessment test Average of two Tests out of Three tests): 15marks.

SCHEME OF EXAMINATION:
Two questions to be set each from Module.
Student has to answer both full questions. 80marks Marks divided in three parts Write up 12marks, Conduction 56marks & Viva 12marks.

12.0 Course Delivery Plan

Experiment	Lecture No.	Content	% of Portion
1.		a) Capture the schematic of CMOS inverter with load capacitance of 0.1pF and set the widths of inverter with Wn = Wp Wn = 2Wp, Wn = Wp/2 and length at selected technology. Carry out the following: a) Set the input signal to a pulse with rise time, fall time of 1ns and pulse width of 10ns and time periodof 20ns and plot the input voltage and output voltage of designed inverter? b) From the simulation results compute tpHL, tpLH and td for all three geometrical settings of width? c). Tabulate the results of delay and find the best geometry for minimum delay for CMOS inverter?	
2.		a) Capture the schematic of 2-input CMOS NAND gate having similar delay as that of CMOS inverter computed in experiment 1. Verify the functionality of NAND gate and also find out the delay td for all four possible combinations of input vectors. Table the results. Increase the drive strength to 2X and 4X and tabulate the results. b)Draw layout of NAND with Wp/Wn = 40/20, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the oservations.	
3.		a) Capture schematic of Common Source Amplifier with PMOS Current Mirror Load and find its transient response and AC response? Measures the Unity Gain Bandwidth (UGB), amplification factor by varying transistor geometries, study the impact of variation in width to UGB. b) Draw layout of common source amplifier, use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations	
4.		a)Capture schematic of two-stage operational amplifier and measure the following: a. UGB b. dB bandwidth c. Gain margin and phase margin with and without coupling capacitance d. Use the op-amp in the inverting and non-inverting configuration and verify its functionality e. Study the UGB, 3dB bandwidth, gain and power requirement in op-amp by varying the stage wise transistor geometries and record the observations. b) Draw layout of two-stage operational amplifier with minimum transistor width set to 300 (in 180/90/45 nm technology), choose appropriate transistor geometries as per the results obtained in 4.a. Use optimum layout methods. Verify for DRC and LVS, extract parasitic and perform post layout simulations, compare the results with pre-layout simulations. Record the observations	

Part – B **Digital Design**			
. 1.	5	1.Write verilog code for 4-bit up/down asynchronous reset counter and carry out the following: a. Verify the functionality using test bench b. Synthesize the design by setting area and timing constraint. Obtain the gate level netlist, find the critical path and maximum frequency of operation. Record the area requirement in terms of number of cells required and properties of each cell in terms of driving strength, power and area requirement. c. Perform the above for 32-bit up/down counter and identify the critical path, delay of critical path, and maximum frequency of operation, total number of cells required and total area.	

2.	6	2.Write verilog code for 4-bit adder and verify its functionality using test bench. Synthesize the design by setting proper constraints and obtain the net list. From the report generated identify critical path, maximum delay, total number of cells, power requirement and total area required. Change the constraints and obtain optimum synthesis results.	
3.	7	Write verilog code for UART and carry out the following: a. Perform functional verification using test bench b. Synthesize the design targeting suitable library and by setting area and timing constraints. c. For various constrains set, tabulate the area, power and delay for the synthesized netlist d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints	
4.	8	Write verilog code for 32-bit ALU supporting four logical and four arithmetic operations, use case statement and if statement for ALU behavioral modeling. a. Perform functional verification using test bench b. Synthesize the design targeting suitable library by setting area and timing constraints c. For various constrains set, tabulate the area, power and delay for the synthesized netlist d. Identify the critical path and set the constraints to obtain optimum gate level netlist with suitable constraints Compare the synthesis results of ALU modeled using IF and CASE statements.	
5.	9	Write verilog code for Latch and Flip-flop, Synthesize the design and compare the synthesis report (D, SR, JK).	
6.	10	For the synthesized netlist carry out the following for any two above experiments: a. Floor planning (automatic), identify the placement of pads b. Placement and Routing, record the parameters such as no. of layers used for routing, flip method for placement of standard cells, placement of standard cells, routes of power and ground, and routing of standard cells c. Physical verification and record the LVS and DRC reports d. Perform Back annotation and verify the functionality of the design e. Generate GDSII and record the number of masks and its color composition	

13.0 VIVA BANK

1. The minimum voltage to keep the MOS transistor in on state is known as
2. 'Pinch off of the channel takes place in which region.
3. Which of 'the following equation is true for liner region?
   a)Vds < Vgs -Vt b) Ids> Vgs - Vt c) Vds = Vgs - Vt d) None
4. The oxide layer used in the MOS fabrication is
5. Which of the following Well process is superior?
   a) P-well b)N-well c) Both P-well and N-well d) None
6. What is the advantage of CMOS technology?
7. Transit time is given by----------
8. When the VTC of the CMOS inverter shifts towards left,
9. The demarcation line has to be drawn in----------stick diagram.
10. If the value of lambda is 1micrometer then the minimum feature size o the transistor is ?
11. The scaling factor for the Gate capacitance Cg is given by
12. The scaling factor for power-speed product is given by
13. If the gate voltage and the input voltage of the NMOS transistor is 5V and threshold voltage of the transistor is O. 7V, then the output voltage
14. The mobility of the electrons is---------- than the holes.
15. As the width of the transistor increases the number of contact cuts----------
16. Transmission gate is----------
17. The CMOS schematic diagram of NAND gate consists of----------
18. If the size of the transistors in an inverter increases, then the input capacitance
19. The minimum value of the scaling factor in a cascaded inverter circuit to drive large capacitive load
20. In a lambda based rules, the distance between two MI layers is
21. Match the following;

A	B
a) CM OS technology	i) Strong '0'
b) Bipolar technology	ii) Strong' 1’
c) Transmission gate	iii) High input impedance

d) PMOS transistor
e) NMOS transistor
iv) Low input impedance
v) Bi-directional switch

22. What is rise time & fall time of Inverter.
23. Define Symmetrical inverter.
24. What is the value of e in case of load handling by invereter.
25. What is Pass transistor?
26. Give the disadvantage of Pass transistor.
27 What is the advantage of Transmission gate over Pass transistor.
28. What is a Flip-flop?
29. What is a master slave Flip-flop?
30. What is a race-around condition?
31. Differentiate Serial & Parallel adder.
32. What is a DAC?
33. Name different types of DAC's.
34. What is a ADC
35. Name different types of ADC's.
36. What is SAR?
37. Explain the working of SAR.
38. What is a Buffer?
39. What is a counter?
40. What is synchronous counter?
41. What is synchronous counter?
42. What is RC extraction?
43. What is Back annotation?
44. What do you mean by DC-analysis?
45. What do you mean by AC-analysis?
46. What is the Gain of common drain amplifier?
47. How the common source amplifier is formed.
48. What is speed Vs area tradeoff?
49. What is the resolution of 4-bit ADC with V reference= 5V
50. What is DRC & ERC.
51. Explain design abstraction for FPGAs.
52. Explain FPGA architecture.
53.Explain in detail the Generic Structure of an FPGA fabric.

14.0 University Result

Examination	FCD	FC	SC	% Passing
Feb 2022	31	03	1	100

Prepared by	Checked by		
Prof. S. S. Kamate	Prof. S. S Patil	HOD	Principal